IN THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1-12. (Canceled)

13. (Currently Amended) A method [[for]] of manufacturing a semiconductor device, comprising the steps of:

forming a gate electrode over a substrate having an insulating surface by discharging a first conductive material;

performing a first heat treatment to the gate electrode by a lamp or a laser beam;

planarizing the gate electrode;

laminating a semiconductor layer, a channel protection layer, and a semiconductor layer having ~~one of~~ n-type or p-type conductivity over the gate electrode;

forming a pixel electrode over the substrate by discharging a second conductive material;

performing a second heat treatment to the pixel electrode by a lamp or a laser beam;

planarizing the pixel electrode;

forming source [[or]] and drain wirings over a semiconductor layer having [[the]] one of n-type or p-type conductivity by discharging a third conductive material; [[and]]

performing a third heat treatment to ~~the gate electrode, and~~ the source and drain wirings by a lamp or a laser beam; and

planarizing the source and drain wirings.

14. (Currently Amended) A method [[for]] of manufacturing a semiconductor device

according to claim 13, wherein the first conductive material and the second conductive material are discharged under reduced pressure.

15. (Currently Amended) A method of manufacturing ~~method of~~ a semiconductor device according to Claim 14, wherein the reduced pressure is 1×10^2 to 2×10^4 Pa.

16. (Currently Amended) A method of manufacturing ~~method of~~ a semiconductor device according to claim 13, wherein said semiconductor device is incorporated into at least one selected from the group consisting of a display device, a personal computer and a portable image reproduction device.

17. (Currently Amended) A method of manufacturing a semiconductor device comprising:

forming a plurality of gate wirings and a plurality of gate electrodes over a substrate by discharging a first conductive material;

performing a first heat treatment to the plurality of gate wirings and the plurality of gate electrodes by a lamp or a laser beam;

planarizing the plurality of gate wirings and the plurality of gate electrodes;

forming an insulating film over the plurality of gate wirings;

laminating a plurality of semiconductor layers, a plurality of channel protection layers, and a plurality of semiconductor layers having ~~one of~~ n-type or p-type conductivity over the insulating film;

forming a plurality of pixel electrodes arranged in a matrix form over the substrate by discharging a second conductive material;

performing a second heat treatment to the plurality of pixel electrodes by a lamp or a laser beam;

planarizing the plurality of pixel electrodes;

forming a plurality of source and drain wirings over the plurality of semiconductor layers having ~~one of~~ n-type or p-type conductivity by discharging a third conductive material wherein said plurality of source and drain wirings extend across said plurality of gate wirings; [[and]]

performing a third heat treatment to the plurality of source and drain wirings by a lamp or a laser beam; and

planarizing the plurality of source and drain wirings.

18. (Currently Amended) A method [[for]] of manufacturing a semiconductor device according to claim 17, wherein the first conductive material, the second conductive material and the third conductive material are discharged under reduced pressure.

19. (Currently Amended) A method of manufacturing ~~method of~~ a semiconductor device according to Claim 18, wherein the reduced pressure is 1×10^2 to 2×10^4 Pa.

20. (Currently Amended) A method of manufacturing ~~method of~~ a semiconductor device according to claim 17, wherein said semiconductor device is incorporated into at least one selected from the group consisting of a display device, a personal computer and a portable image reproduction device.

21. (Currently Amended) A method of manufacturing a semiconductor device comprising:

forming a plurality of gate wirings and a plurality of gate electrodes over a substrate by discharging a first conductive material;

performing a first heat treatment to the plurality of gate wirings and the plurality of gate electrodes by a lamp or a laser beam;

planarizing the plurality of gate wirings and the plurality of gate electrodes;

forming a first insulating film over the plurality of gate wirings;

laminating a plurality of semiconductor layers, a plurality of channel protection layers, and a plurality of semiconductor layers having ~~one of~~ n-type or p-type conductivity over the first insulating film;

forming a plurality of pixel electrodes arranged in a matrix form over the substrate by discharging a second conductive material;

performing a second heat treatment to the plurality of pixel electrodes by a lamp or a laser beam;

planarizing the plurality of pixel electrodes;

forming a plurality of source and drain wirings over the plurality of semiconductor layers having ~~one of~~ n-type or p-type conductivity by discharging a third conductive material wherein said plurality of source and drain wirings extend across said plurality of gate wirings;

performing a third heat treatment to the plurality of source and drain wirings by a lamp or a laser beam; [[and]]

planarizing the plurality of source and drain wirings; and

forming a second insulating film over the plurality of source and drain wirings.

22. (Currently Amended) A method [[for]] of manufacturing a semiconductor device

according to claim 21, wherein the first conductive material, the second conductive material and the third conductive material are discharged under reduced pressure.

23. (Currently Amended) A method of manufacturing ~~method of~~ a semiconductor device according to Claim 22, wherein the reduced pressure is 1×10^2 to 2×10^4 Pa.

24. (Currently Amended) A method of manufacturing ~~method of~~ a semiconductor device according to claim 21, wherein said semiconductor device is incorporated into at least one selected from the group consisting of a display device, a personal computer and a portable image reproduction device.

25. (Currently Amended) A method of manufacturing a semiconductor device comprising:

forming a semiconductor island over a substrate;

forming an insulating film over the semiconductor island;

forming a gate electrode and a gate wiring by discharging a first conductive material;

performing a first heat treatment to the gate wiring and the gate electrode by a lamp or a laser beam;

planarizing the gate electrode and the gate wiring;

doping an impurity element having a conductive type of n-type or p-type into the semiconductor island using the gate electrode as a mask;

forming an interlayer insulating film over the gate electrode;

forming source and drain wirings over the interlayer insulating film by discharging a second conductive material; [[and]]

performing a second heat treatment to the source and drain wirings by a lamp or a laser beam;

planarizing the source and drain wirings;

forming a first electrode over the source and drain wirings by discharging a third conductive material; [[and]]

performing a third heat treatment to the first electrode by a lamp or a laser beam; and

planarizing the first electrode.

26. (Currently Amended) A method [[for]] of manufacturing a semiconductor device according to claim 25, wherein the first conductive material, the second conductive material and the third conductive material are discharged under reduced pressure.

27. (Currently Amended) A method of manufacturing ~~method of~~ a semiconductor device according to Claim [[25]] 26, wherein the reduced pressure is 1×10^2 to 2×10^4 Pa.

28. (Currently Amended) A method of manufacturing ~~method of~~ a semiconductor device according to claim 25, wherein said semiconductor device is incorporated into at least one selected from the group consisting of a display device, a personal computer and a portable image reproduction device.

29. (Currently Amended) A method of manufacturing ~~method of~~ a semiconductor device according to claim 25, ~~wherein the method~~ further comprising:

forming an electroluminescent layer by discharging an electroluminescent ~~a fourth conductive~~ material; and

forming a second electrode over the electroluminescent layer by discharging a [[fifth]] fourth conductive material.

30. (Currently Amended) A method of manufacturing ~~method of~~ a semiconductor device according to claim 25, wherein the semiconductor island is an amorphous silicon.

31. (Currently Amended) A method of manufacturing ~~method of~~ a semiconductor device according to claim 25, wherein the first electrode is an anode electrode.

32. (Currently Amended) A method of manufacturing a semiconductor device comprising:

forming a semiconductor island over a substrate;

forming an insulating film over the semiconductor island;

forming a gate electrode and a gate wiring by discharging a first conductive material, wherein the gate electrode is formed by discharging the first conductive material from a first ink-jet unit while the gate wiring is formed by discharging the first conductive material from a second ink-jet unit;

performing a first heat treatment to the gate wiring and the gate electrode by a lamp or a laser beam;

planarizing the gate wiring and the gate electrode;

doping an impurity element having a conductive type of n-type or p-type into the semiconductor island using the gate electrode as a mask;

forming an interlayer insulating film over the gate electrode;

forming source and drain wirings over the interlayer insulating film by discharging a second

conductive material;

performing a second heat treatment to the source and drain wirings by a lamp or a laser beam;

planarizing the source and drain wirings;

forming a first electrode over the source and drain wirings by discharging a third conductive material wherein first electrode is formed by discharging the third conductive material from the second ink-jet unit; [[and]]

performing a third heat treatment to the first electrode by a lamp or a laser beam[[,]]; and

planarizing the first electrode,

wherein the number of ink-heads provided in the second ink-jet unit is larger than that provided in the first ink-jet unit.

33. (Currently Amended) A method [[for]] of manufacturing a semiconductor device according to claim 32, wherein the first conductive material, the second conductive material and the third conductive material are discharged under reduced pressure.

34. (Currently Amended) A method of manufacturing ~~method of~~ a semiconductor device according to Claim [[32]] 33, wherein the reduced pressure is 1×10^2 to 2×10^4 Pa.

35. (Currently Amended) A method of manufacturing ~~method of~~ a semiconductor device according to claim 32, wherein said semiconductor device is incorporated into at least one selected from the group consisting of a display device, a personal computer and a portable image reproduction device.

36. (Currently Amended) A method of manufacturing ~~method of~~ a semiconductor device according to claim 32, ~~wherein the method~~ further comprising:

forming an electroluminescent layer by discharging an electroluminescent ~~a fourth conductive~~ material; and

forming a second electrode over the electroluminescent layer by discharging a [[fifth]] fourth conductive material.

37. (Currently Amended) A method of manufacturing ~~method of~~ a semiconductor device according to claim 32, wherein the semiconductor island is an amorphous silicon.

38. (Currently Amended) A method of manufacturing ~~method of~~ a semiconductor device according to claim 32, wherein the first electrode is an anode electrode.

39. (Currently Amended) A method of manufacturing a semiconductor device comprising:

forming a plurality of semiconductor islands over the substrate;

forming an insulating film over the plurality of semiconductor islands;

forming a plurality of gate wirings, and a plurality of gate electrodes by discharging a first conductive material;

performing a first heat treatment to the plurality of gate wirings and the plurality of gate electrodes by a lamp or a laser beam;

planarizing the plurality of gate wirings and the plurality of gate electrodes;

doping an impurity element having a conductive type of n-type or p-type into the plurality of semiconductor islands using the plurality of gate electrodes as a mask;

forming an interlayer insulating film over the plurality of gate electrodes;

forming a plurality of source and drain wirings over the interlayer insulating film by discharging a second conductive material;

performing a second heat treatment to the plurality of source and drain wirings by a lamp or a laser beam;

planarizing the plurality of source and drain wirings;

forming a plurality of first electrodes arranged in a matrix form over the plurality of source and drain wirings by discharging a third conductive material; [[and]]

performing a third heat treatment to the plurality of first electrodes by a lamp or a laser beam; and

planarizing the plurality of first electrodes.

40. (Currently Amended) A method [[for]] of manufacturing a semiconductor device according to claim 39, wherein the first conductive material, the second conductive material and the third conductive material are discharged under reduced pressure.

41. (Currently Amended) A method of manufacturing ~~method of~~ a semiconductor device according to Claim [[39]] 40, wherein the reduced pressure is 1×10^2 to 2×10^4 Pa.

42. (Currently Amended) A method of manufacturing ~~method of~~ a semiconductor device according to claim 39, wherein said semiconductor device is incorporated into at least one selected from the group consisting of a display device, a personal computer and a portable image reproduction device.

43. (Currently Amended) A method of manufacturing ~~method of~~ a semiconductor device according to claim 39, ~~wherein the method~~ further comprising:

forming a plurality of electroluminescent layers by discharging an electroluminescent ~~a fourth conductive~~ material; and

forming a plurality of a second electrode over the plurality of electroluminescent layers by discharging a [[fifth]] fourth conductive material.

44. (Currently Amended) A method of manufacturing ~~method of~~ a semiconductor device according to claim 39, wherein the plurality of semiconductor islands is an amorphous silicon.

45. (Currently Amended) A method of manufacturing ~~method of~~ a semiconductor device according to claim 39, wherein the plurality of first electrodes is an anode electrode.

46. (Currently Amended) A method of manufacturing a semiconductor device comprising:

forming a plurality of semiconductor islands over the substrate;

forming an insulating film over the plurality of semiconductor islands;

forming a plurality of gate wirings, and a plurality of gate electrodes by discharging a first conductive material, wherein the plurality of gate electrodes are formed by discharging the first conductive material from a first ink-jet unit while the plurality of gate wirings are formed by discharging the first conductive material from a second ink-jet unit;

performing a first heat treatment to the plurality of gate wirings and the plurality of gate electrodes by a lamp or a laser beam;

planarizing the plurality of gate wirings and the plurality of gate electrodes;

doping an impurity element having a conductive type of n-type or p-type into the plurality of semiconductor islands using the plurality of gate electrodes as a mask;

forming an interlayer insulating film over the plurality of gate electrodes;

forming a plurality of source and drain wirings over the interlayer insulating film by discharging a second conductive material;

performing a second heat treatment to the plurality of source and drain wirings by a lamp or a laser beam;

planarizing the plurality of source and drain wirings;

forming a plurality of first electrodes arranged in a matrix form over the plurality of source and drain wirings by discharging a third conductive material, wherein plurality of first electrodes are formed by discharging the third conductive material from the second ink-jet unit; [[and]]

performing a third heat treatment to the plurality of first electrodes by a lamp or a laser beam; and

planarizing the plurality of gate wirings and the plurality of gate electrodes,

wherein the number of ink-heads provided in the second ink-jet unit is larger than that provided in the first ink-jet unit.

47. (Currently Amended) A method [[for]] of manufacturing a semiconductor device according to claim 46, wherein the first conductive material, the second conductive material and the third conductive material are discharged under reduced pressure.

48. (Currently Amended) A method of manufacturing ~~method of~~ a semiconductor device

according to Claim [[46]] 47, wherein the reduced pressure is 1×10^2 to 2×10^4 Pa.

49. (Currently Amended) A method of manufacturing ~~method of~~ a semiconductor device according to claim 46, wherein said semiconductor device is incorporated into at least one selected from the group consisting of a display device, a personal computer and a portable image reproduction device.

50. (Currently Amended) A method of manufacturing ~~method of~~ a semiconductor device according to claim 46, wherein the method further comprising:

forming a plurality of electroluminescent layers by discharging an electroluminescent ~~a fourth conductive~~ material; and

forming a plurality of a second electrode over the plurality of electroluminescent layers by discharging a [[fifth]] fourth conductive material.

51. (Currently Amended) A method of manufacturing ~~method of~~ a semiconductor device according to claim 46, wherein the plurality of semiconductor islands is an amorphous silicon.

52. (Currently Amended) A method of manufacturing ~~method of~~ a semiconductor device according to claim 46, wherein the plurality of first electrode is an anode electrode.

53. (Currently Amended) A method of manufacturing ~~method of~~ a semiconductor device according to claim 13, wherein the second conductive material is dissolved or dispersed in a solvent.

54. (Currently Amended) A method of manufacturing ~~method of~~ a semiconductor device according to claim 17, wherein the second conductive material is dissolved or dispersed in a solvent.

55. (Currently Amended) A method of manufacturing ~~method of~~ a semiconductor device according to claim 21, wherein the second conductive material is dissolved or dispersed in a solvent.

56. (Currently Amended) A method of manufacturing ~~method of~~ a semiconductor device according to claim 25, wherein the third conductive material is dissolved or dispersed in a solvent.

57. (Currently Amended) A method of manufacturing ~~method of~~ a semiconductor device according to claim 32, wherein the third conductive material is dissolved or dispersed in a solvent.

58. (Currently Amended) A method of manufacturing ~~method of~~ a semiconductor device according to claim 39, wherein the third conductive material is dissolved or dispersed in a solvent.

59. (Currently Amended) A method of manufacturing ~~method of~~ a semiconductor device according to claim 46, wherein the third conductive material is dissolved or dispersed in a solvent.

60. (Currently Amended) A method of manufacturing ~~method of~~ a semiconductor device according to claim 13, wherein the pixel electrode comprises at least one material selected from the group consisting of a compound of indium oxide and tin oxide, a compound of indium oxide and zinc oxide, zinc oxide, tin oxide, indium oxide and titanium oxide.

61. (Currently Amended) A method of manufacturing ~~method of~~ a semiconductor device according to claim 17, wherein each of the plurality of pixel electrodes comprises at least one material selected from the group consisting of a compound of indium oxide and tin oxide, a compound of indium oxide and zinc oxide, zinc oxide, tin oxide, indium oxide and titanium oxide.

62. (Currently Amended) A method of manufacturing ~~method of~~ a semiconductor device according to claim 21, wherein each of the plurality of pixel electrodes comprises at least one material selected from the group consisting of a compound of indium oxide and tin oxide, a compound of indium oxide and zinc oxide, zinc oxide, tin oxide, indium oxide and titanium oxide.

63. (Currently Amended) A method of manufacturing ~~method of~~ a semiconductor device according to claim 25, wherein the first electrode comprises at least one material selected from the group consisting of a compound of indium oxide and tin oxide, a compound of indium oxide and zinc oxide, zinc oxide, tin oxide, indium oxide and titanium oxide.

64. (Currently Amended) A method of manufacturing ~~method of~~ a semiconductor device according to claim 32, wherein the first electrode comprises at least one material selected from the group consisting of a compound of indium oxide and tin oxide, a compound of indium oxide and zinc oxide, zinc oxide, tin oxide, indium oxide and titanium oxide.

65. (Currently Amended) A method of manufacturing ~~method of~~ a semiconductor device according to claim 39, wherein each of the plurality of first electrodes comprises at least one material selected from the group consisting of a compound of indium oxide and tin oxide, a compound of

indium oxide and zinc oxide, zinc oxide, tin oxide, indium oxide and titanium oxide.

66. (Currently Amended) A method of manufacturing ~~method of~~ a semiconductor device according to claim 46, wherein each of the plurality of first electrodes comprises at least one material selected from the group consisting of a compound of indium oxide and tin oxide, a compound of indium oxide and zinc oxide, zinc oxide, tin oxide, indium oxide and titanium oxide.

67. (New) A method of manufacturing a semiconductor device according to claim 13, wherein the gate electrode is formed by discharging the first conductive material in sequence, the pixel electrode is formed by discharging the second conductive material in sequence, and the source and drain wirings are formed by discharging the third conductive material in sequence.

68. (New) A method of manufacturing a semiconductor device according to claim 17, wherein the plurality of gate wirings and the plurality of gate electrodes are formed by discharging the first conductive material in sequence, the plurality of the pixel electrodes are formed by discharging the second conductive material in sequence, and the plurality of source and drain wirings are formed by discharging the third conductive material in sequence.

69. (New) A method of manufacturing a semiconductor device according to claim 21, wherein the plurality of gate wirings and the plurality of gate electrodes are formed by discharging the first conductive material in sequence, the plurality of the pixel electrodes are formed by discharging the second conductive material in sequence, and the plurality of source and drain wirings are formed by discharging the third conductive material in sequence.

70. (New) A method of manufacturing a semiconductor device according to claim 25, wherein the gate electrode and the gate wiring are formed by discharging the first conductive material in sequence, the source and drain wirings are formed by discharging the second conductive material in sequence, and the first electrode is formed by discharging the third conductive material in sequence.

71. (New) A method of manufacturing a semiconductor device according to claim 32, wherein the gate electrode and the gate wiring are formed by discharging the first conductive material in sequence, the source and drain wirings are formed by discharging the second conductive material in sequence, and the first electrode is formed by discharging the third conductive material in sequence.

72. (New) A method of manufacturing a semiconductor device according to claim 39, wherein the plurality of gate wirings and the plurality of gate electrodes are formed by discharging the first conductive material in sequence, the plurality of source and drain wirings are formed by discharging the second conductive material in sequence, and the plurality of first electrodes are formed by discharging the third conductive material in sequence.

73. (New) A method of manufacturing a semiconductor device according to claim 46, wherein the plurality of gate wirings and the plurality of gate electrodes are formed by discharging the first conductive material in sequence, the plurality of source and drain wirings are formed by

discharging the second conductive material in sequence, and the plurality of first electrodes are formed by discharging the third conductive material in sequence.